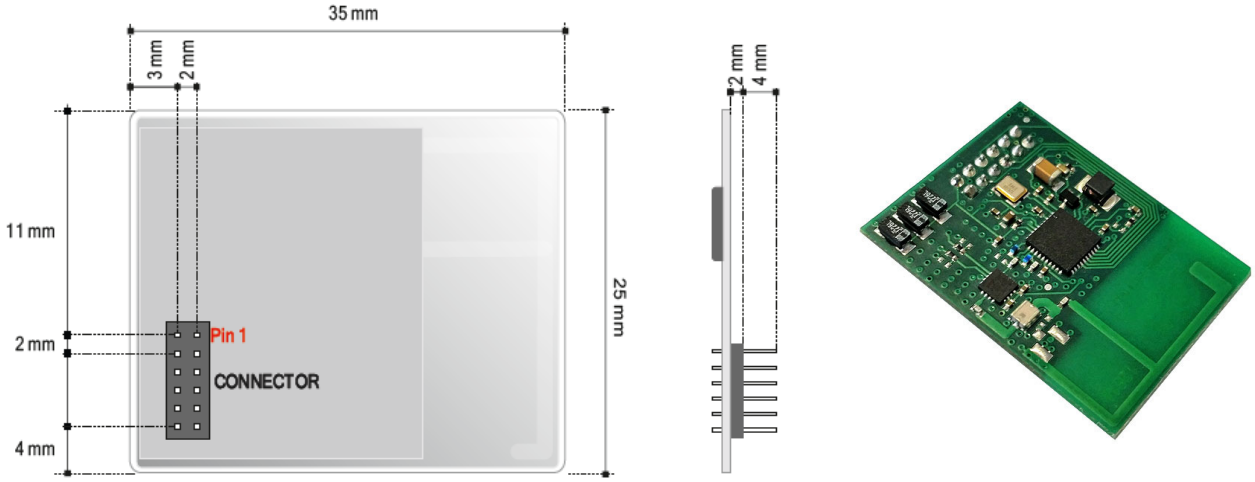
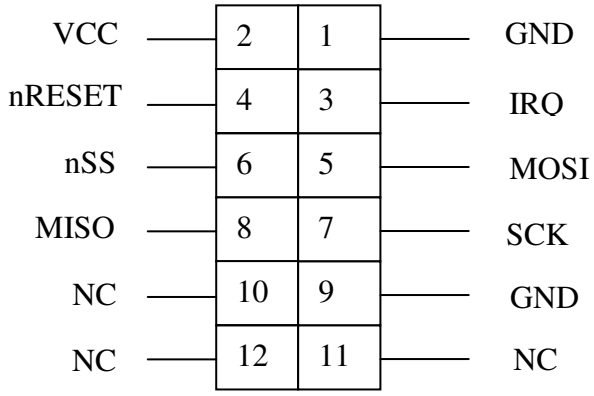
General description:



Long range transceiver XTR VF 2.4 HP/H-AI is pin-to-pin compatible with previous model XTR VF 2.4 LP, representing an extension suitable to reach a RF output power (ERP) increate up to 20dBm (compared with the 4 dBm of the XTR VF 2.4 LP). In this way it's possible to cover in open space outdoor conditions, a radio link of 200 meters.
Radio transceiver embeds an integrated PIFA (Planar Inverted F Antenna) antenna.
In case the final application needs to use a battery powered device, and a very low power steady consumption, XTR VF 2.4 HP/H-AI is fully compatible simply by providing some additions to the firmware (see dedicated paragraph).
It operates in the License Free Industrial, Scientific and Medical (ISM) band at 2.4GHz and it offers a complete radio module solution for integration into existing or new 2.4GHz products. It uses a DSSS (Direct Sequence Spread Spectrum) technique that allows operation in disturbed environments and that reduces the interference caused by traditional narrowband signals. This technique also allows coexistence with Bluetooth and Wi-Fi as well as all other wireless technologies that utilize the 2.4GHz ISM Band.
Transceiver embeds a power amplifier (PA) for transmission, and a Low Noise Amplifier (LNA) to clear up the signal received. Module can be connected to a microcontroller and one or more external devices via SPI Interface. This last facility makes possible full transceiver programmability: in particular, possibility is given to set RF channel, data transmission speed and RF radiated power level.
Thanks to the power amplifier, output power could achieve +20 dBm (step from -10 to +20dBm). RF channels available are 98 (1 MHz wide channels, from 2.400 to 2.497GHz), available, for usage compliant to national requirements, in the ISM band of 2.400 to 2.4835GHz Band.
Transmission data rate is selectable from 16Kbit/sec to 250Kbit/sec according to the used spreading code. It can be increased to 1Mbit/sec if spread spectrum technique is not used.

Pin out



Pin out description

Pin		Description
1,9	GND	GND connection
2	VCC	Positive Voltage supply connection
3	IRQ	Interrupt signal from the radio module to an external microcontroller
4	nRESET	Reset signal (active high) from an external microcontroller to the radio module
5	MOSI	Master Out Slave In. SPI signal from an external microcontroller to the radio module.
6	nSS	Slave Select signal (active low) from an external microcontroller to the radio module
7	SCK	SPI clock from an external microcontroller to the radio module
8	MISO	Master In Slave Out. SPI signal from the radio module to an external microcontroller

Reference Documentation

The XTR VF 2.4 HP/H-AI modules use the Cypress Semiconductor CYRF6936 LP 2.4GHz DSSS Radio SOC device.
For information on technical details of the Cypress Semiconductor, CYRF6936 LP 2.4GHz DSSS Radio SOC such as register settings, timing, application interfaces and clocking, refer to the device data sheet available on the Cypress Web Site at: www.cypress.com

The following is the link location of CYRF6936 LP 2.4GHz DSSS Radio SOC documentation known at the time of publication of this data sheet:
http://www.cypress.com/?mpn=CYRF6936-40LTXC

See also Aurel AN0003 application note available on Aurel web site.
This application note contains a description of register settings to initialize CYRF6936 and to perform basic transmission and reception of a packet.

Firmware additions compared with the previous module Aurel XTR VF 2.4 LP

XTR VF 2.4 HP/H-AI, compared to the previous module XTR VF 2.4 LP, introduces a power amplifier (PA) and a Low Noise Amplifier (LNA). These additional components are managed inside the module itself through the lines PACTL/GPIO (pin 30) e XOUT/GPIO (pin 29) of the CYRF6936.
Therefore, it's necessary to program the CYRF6936 to use these lines as GPIO and drive them properly.
At device initialization time, it's necessary to setup XOUT and PACTL as GPIO and setup as low output as follow:

Setting XOUT as GPI0:

Register 0x0C => Bit 6 = Bit 7 = 1

Setting PACTL as GPIO:

Register 0x0D => Bit 2 = 1

Setting XOUT and PACTL as standard CMOS Output

Register 0x0D => Bit 3 = Bit 4 = 0

Output setting XOUT and PACTL to value 0:

Register 0x0E => Bit 5 = Bit 7 = 0

XOUT and PACTL management is different depending if device is in transmission, in reception or in power down, as follow:

Transmission

Before to activate the transmission, it's necessary to switch on the Power amplifier.
Therefore before to lift up TX GO bit on register 0x02, it's necessary perform the following operation:

Register 0x0E => Bit 5 = Bit 7 = 1 meaning PACTL and XOUT = 1

Reception

Before to activate the reception, it's necessary to switch on the Low Noise Amplifier.
Therefore before to lift up RX GO bit on register 0x05, it's necessary perform the following operation:

Register 0x0E => Bit 5 = 0 , Bit 7 = 1 meaning PACTL = 0 and XOUT = 1

Power Down

In order to obtain a low consumption, it's necessary disable both PA and LNA. Therefore before to put the device in power down or Idle mode, it's necessary perform the following operation:

Register 0x0E => Bit 5 = Bit 7 = 0 meaning PACTL = XOUT = 0

European Reference Standards

The module **XTR VF 2.4 HP/H-AI** complies with the European standards **EN 300-228**, **EN 300-440** and **EN 301-489** with maximum power supply of 3.6V. The product has been tested according to EN 60950 and can be used inside a special housing that ensures compliance with the above mentioned regulations. The device must be powered by a low voltage safety source protected against short circuits.

The use of the module is foreseen inside housings that assure the overcoming of standards EN 61000 not directly applicable to the module itself. In particular, it is the user's care isolation antenna as the RF output of the transmitter is not able to support directly the electrostatic charges foreseen by the standard EN 61000-4-2.

Functional Overview

The XTR VF 2.4 HP/H-AI module is designed to implement wireless device links operating in the worldwide 2.4-GHz ISM frequency band. It is intended for systems compliant with world-wide regulations covered by Europe ETSI EN 301 489, ETSI EN300 440, ETSI EN 300 328 and USA FCC Part 15.
The module contains a 2.4-GHz 1-Mbps GFSK radio transceiver, packet data buffering, packet framer, DSSS baseband controller, Received Signal Strength Indication (RSSI), and SPI interface for data transfer and device configuration.
The radio supports 98 discrete 1-MHz channels (regulations may limit the use of some of these channels in certain jurisdictions).
In DSSS modes the baseband performs DSSS spreading/de-spreading, while in GFSK Mode (1 Mb/s - GFSK) the baseband performs Start of Frame (SOF), End of Frame (EOF) detection and CRC16 generation and checking. The baseband may also be configured to automatically transmit Acknowledge (ACK) handshake packets whenever a valid packet is received.
When in receive mode, with packet framing enabled, the device is always ready to receive data transmitted at any of the supported bit rates, except SDR, enabling the implementation of mixed-rate systems in which different devices use different data rates. This also enables the implementation of dynamic data rate systems, which use high data rates at shorter distances and/or in a low-moderate interference environment, and change to lower data rates at longer distances and/or in high interference environments.
In addition, the XTR VF 2.4 HP/H-AI has a Power Management Unit (PMU), which enables direct connection of the device to any battery voltage in the range 2.0 V to 3.6 V. The PMU conditions the battery voltage to provide the supply voltages required by the device, and may supply external devices.

Link Layer Modes

The XTR VF 2.4 HP/H-AI module supports the following data packet framing features:

SOP
Packets begin with a 2-symbol Start of Packet (SOP) marker. This is required in GFSK and 8DR modes, but is optional in DDR mode and is not supported in SDR mode; if framing is disabled then an SOP event is inferred whenever two successive correlations are detected. The SOP_CODE_ADR code used for the SOP is different from that used for the "body" of the packet and if desired may be a different length. SOP must be configured to be the same length on both sides of the link.

Lenght
There are two options for detecting the end of a packet. If SOP is enabled, then a packet length field may be enabled. GFSK and 8DR must enable the length field. This is the first 8-bits after the SOP symbol, and is transmitted at the payload data rate. If the length field is enabled, an End of Packet (EOP) condition is inferred after reception of the number of bytes defined in the length field, plus two bytes for the CRC16 (if enabled). The alternative to using the length field is to infer an EOP condition from a configurable number of successive non-correlations; this option is not available in GFSK mode and is only recommended to enable when using SDR mode.

CRC16
The device may be configured to append a 16-bit CRC16 to each packet. The CRC16 uses the USB CRC polynomial with the added programmability of the seed. If enabled, the receiver will verify the calculated CRC16 for the payload data against the received value in the CRC16 field. The starting value for the CRC16 calculation is configurable, and the CRC16 transmitted may be calculated using either the loaded seed value or a zero seed; the received data CRC16 will be checked against both the configured and zero CRC16 seeds.
CRC16 detects the following errors:

- any one bit in error
- any two bits in error (no matter how far apart, which column, and so on)
- any odd number of bits in error (no matter where they are)
- an error burst as wide as the checksum itself

Packet Buffers

All data transmission and reception utilizes the 16-byte packet buffers, one for transmission and one for reception.
The transmit buffer allows a complete packet of up to 16-bytes of payload data to be loaded in one burst SPI transaction, and then transmitted with no further microcontroller intervention. Similarly, the receive buffer allows an entire packet of payload data up to 16 bytes to be received with no firmware intervention required until packet reception is complete.
The XTR VF 2.4 HP/H-AI module supports packet length of up to 40 bytes; interrupts are provided to allow a microcontroller to use the transmit and receive buffers as FIFOs. When transmitting a packet longer than 16 bytes, the microcontroller can load 16-bytes initially, and add further bytes to the transmit buffer as transmission of data creates space in the buffer. Similarly, when receiving packets longer than 16 bytes, the microcontroller must fetch received data from the FIFO periodically during packet reception to prevent it from overflowing.

Auto Transaction Sequencer (ATS)

The XTR VF 2.4 HP/H-AI module provides automated support for transmission and reception of acknowledged data packets.
When transmitting a data packet, the device automatically starts the crystal and synthesizer, enters transmit mode, transmits the packet in the transmit buffer, and then automatically switches to receive mode and waits for a handshake packet and then automatically reverts to sleep mode or idle mode when either an ACK packet is received, or a timeout period expires.
Similarly, when receiving in transaction mode, the device waits in receive mode for a valid packet to be received, and then automatically transitions to transmit mode, transmits an ACK packet, and then switches back to receive mode to await the next packet. The contents of the packet buffers are not affected by the transmission or reception of ACK packets.
In each case, the entire packet transaction takes place without any need for microcontroller firmware action; to transmit data the micro controller simply needs to load the data packet to be transmitted, set the length, and set the TX GO bit. Similarly, when receiving packets in transaction mode, firmware simply needs to retrieve the fully received packet in response to an interrupt request indicating reception of a packet.

Data Rates

The XTR VF 2.4 HP/H-AI module supports the following data rates by combining the PN code lengths and data transmission modes:
- 1000 kbps (GFSK)
- 250 kbps (32 chip 8DR)
- 125 kbps (64 chip 8DR)
- 62.5 kbps (32 chip DDR)
- 31.25 kbps (64 chip DDR)
- 15.625 kbps (64 chip SDR)

SPI Communication

The XTR VF 2.4 HP/H-AI has an SPI interface supporting communications between an application microcontroller and one or more slave devices. The SPI interface supports single-byte and multi-byte serial transfers using either 4-pin or 3-pin interfacing. The SPI communications interface consists of Slave Select (nSS), Serial Clock (SCK), and Master Out-Slave In (MOSI), Master In-Slave Out (MISO), or Serial Data (SDAT).
The SPI communications is as follows:
- Command Direction (bit 7) = "1" enables SPI write transaction. A "0" enables SPI read transactions.
- Command Increment (bit 6) = "1" enables SPI auto address increment. When set, the address field automatically increments at the end of each data byte in a burst access, otherwise the same address is accessed.
- Six bits of address.
- Eight bits of data.

The device receives SCK from an application microcontroller on the SCK pin. Data from the application microcontroller is shifted in on the MOSI pin. Data to the application microcontroller is shifted out on the MISO pin. The active-low Slave Select (nSS) pin must be asserted to initiate an SPI transfer.
The application microcontroller can initiate SPI data transfers via a multi byte transaction. The first byte is the Command/Address byte, and the following bytes are the data bytes as shown in Figure 1 through Figure 5.
The SPI communications interface has a burst mechanism, where the first byte can be followed by as many data bytes as desired. A burst transaction is terminated by deasserting the slave select (nSS = 1).

The SPI communications interface single read and burst read sequences are shown in Figure 2 and Figure 3, respectively.
The SPI communications interface single write and burst write sequences are shown in Figure 4 and Figure 5, respectively.
This interface may optionally be operated in a 3-pin mode with the MISO and MOSI functions combined in a single bidirectional data pin (SDAT).
When using 3-pin mode, user firmware should ensure that the MOSI pin on the microcontroller is in a high impedance state except when MOSI is actively transmitting data.
The device registers may be written to or read from 1 byte at a time, or several sequential register locations may be written/read in a single SPI transaction using incrementing burst mode. In addition to single byte configuration registers, the device includes register files; register files are FIFOs written to and read from using non-incrementing burst SPI transactions.
The IRQ pin function may optionally be multiplexed onto the MOSI pin; when this option is enabled the IRQ function is not available while the nSS pin is low. When using this configuration, user firmware should ensure that the MOSI pin on the XTR VF 2.4 HP/H-AI is in a high impedance state whenever the nSS pin is high.
The SPI interface is not dependent on the internal 12-MHz clock, and registers may therefore be read from or written to while the device is in sleep mode, and the 12-MHz oscillator disabled.

Parameter	Byte 1			Byte 1+N
Bit #	7	6	[5:0]	[7:0]
Bit Name	DIR	INC	Address	Data

Figure 1 – SPI Transaction Format

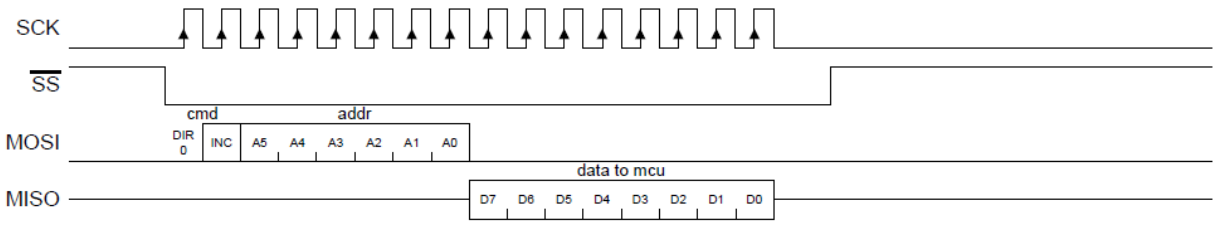


Figure 2 – SPI Single Read Sequence

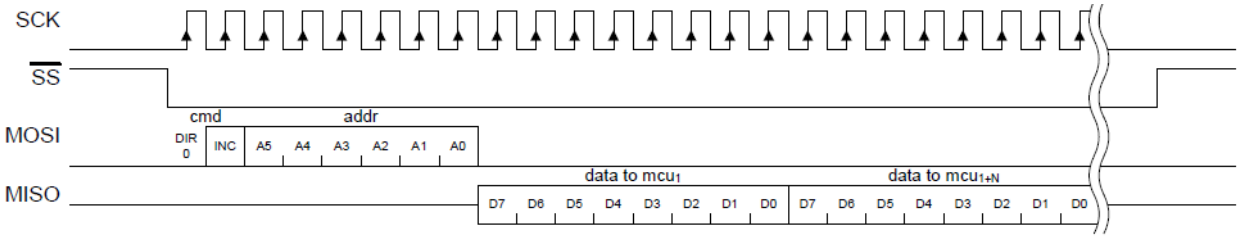


Figure 3 – SPI Incrementing Burst Read Sequence

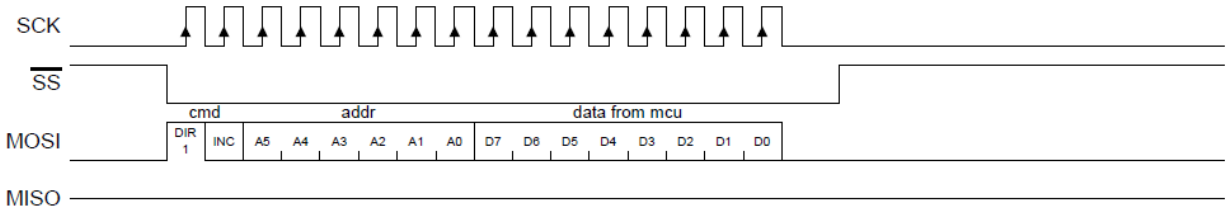


Figure 4 – SPI Single Write Sequence

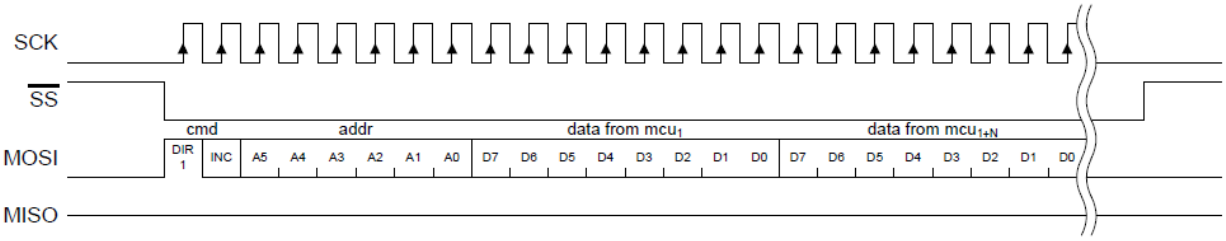


Figure 5 – SPI Incrementing Burst Write Sequence

Interrupts

The device provides an interrupt (IRQ) output, which is configurable to indicate the occurrence of various different events. The IRQ pin may be programmed to be either active HIGH or active LOW, and be either a CMOS or open drain output.
The XTR VF 2.4 HP/H-AI features three sets of interrupts: transmit, receive, and system interrupts. These interrupts all share a single pin (IRQ), but can be independently enabled or disabled.
The contents of the enable registers are preserved when switching between transmit and receive modes.
If more than one interrupt is enabled at any time, it is necessary to read the relevant status register to determine which event caused the IRQ pin to assert. Even when a given interrupt source is disabled, the status of the condition that would otherwise cause an interrupt can be determined by reading the appropriate status register. It is therefore possible to use the devices without the IRQ pin, by polling the status registers to wait for an event, rather than using the IRQ pin.

Power Management

The operating voltage of the module is 2.0V to 3.6V DC, which is applied to the Vcc pin 2 of the connector. The device can be shut down to a fully static sleep mode by writing to the FRC END = 1 and END STATE = 000 bits in the XACT_CFG_ADR register over the SPI interface. The module will enter sleep mode within 35-µs after the last SCK positive edge at the end of this SPI transaction. Alternatively, the module may be configured to automatically enter sleep mode after completing packet transmission or reception. When in sleep mode, the on-chip oscillator is stopped, but the SPI interface remains functional.
The module will wake from sleep mode automatically when the module is commanded to enter transmit or receive mode.
When resuming from sleep mode, there is a short delay while the oscillator restarts. The module may be configured to assert the IRQ pin when the oscillator has stabilized.

Low Noise Amplifier (LNA) and Received Signal Strength Indication (RSSI)

The gain of the receiver may be controlled directly by clearing the AGC EN bit and writing to the Low Noise Amplifier (LNA) bit of the RX_CFG_ADR register. When the LNA bit is cleared, the receiver gain is reduced by approximately 20 dB, allowing accurate reception of very strong received signals (for example when

operating a receiver very close to the transmitter). Approximately 30 dB of receiver attenuation can be added by setting the Attenuation (ATT) bit; this allows data reception to be limited to devices at very short ranges. Disabling AGC and enabling LNA is recommended unless receiving from a device using external PA.
When the module is in receive mode the RSSI_ADR register returns the relative signal strength of the on-channel signal power.
When receiving, the module will automatically measure and store the relative strength of the signal being received as a 5 bit value.
An RSSI reading is taken automatically when the SOP is detected. In addition, a new RSSI reading is taken every time the previous reading is read from the RSSI_ADR register, allowing the background RF energy level on any given channel to be easily measured when RSSI is read when no signal is being received. A new reading can occur as fast as once every 12 µs.

Operating Conditions

VCC	2.0V to 3.6V
TA(Ambient Temperature under Bias)	0°C to +70°C

DC Characteristics (T = 25°C, Vcc = 2.4V)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
Vcc	Power supply voltage	0 to 70°C	2.0		3.6	V
I synth	Icc during synth start			8.4		mA
Tx Icc7	Icc during transmit	PA step 7 (+20dBm)		160		mA
Tx Icc6	Icc during transmit	PA step 6 (+18dBm)		135		mA
Tx Icc5	Icc during transmit	PA step 5 (16dBm)		90		mA
Tx Icc4	Icc during transmit	PA step 4 (11dBm)		55		mA
Rx Icc	Icc during receive			31		mA
Sleep Icc	Icc during sleep mode			2	11	uA
Sleep Icc PMU	Icc during sleep mode	PMU enabled		32		uA

AC Characteristics

SPI interface

Parameter	Description	Min.	Typ.	Max.	Unit
t_{SCK_CYC}	SPI Clock period	238.1			ns
t_{SCK_HI}	SPI Clock High Time	100			ns
t_{SCK_LO}	SPI Clock Low Time	100			ns
t_{DAT_SU}	SPI Input Data Set-up Time	25			ns
t_{DAT_HLD}	SPI Input Data Hold Time	10			ns
t_{DAT_VAL}	SPI Output Data Valid Time	0		50	ns
$t_{DAT\_VAL\_TRI}$	SPI Output Data Tri-state (MOSI from nSS deasserted)			20	ns
t_{SS_SU}	SPI nSS Setup Time before first positive edge of SCK [1]	10			ns
t_{SS_HLD}	SPI Slave Select Hold Time after last negative edge of SCK	10			ns
t_{SS_PW}	SPI Slave Select Minimum Pulse Width	20			ns
t_{SCK_SU}	SPI Slave Select Setup Time	10			ns
t_{SCK_HOLD}	SPI SCK Hold Time	10			ns
t_{RESET}	Minimum RST Pin Pulse Width	10			ns

[1] SCK must start low at the time nSS goes low, otherwise the success of SPI transaction is not guaranteed.

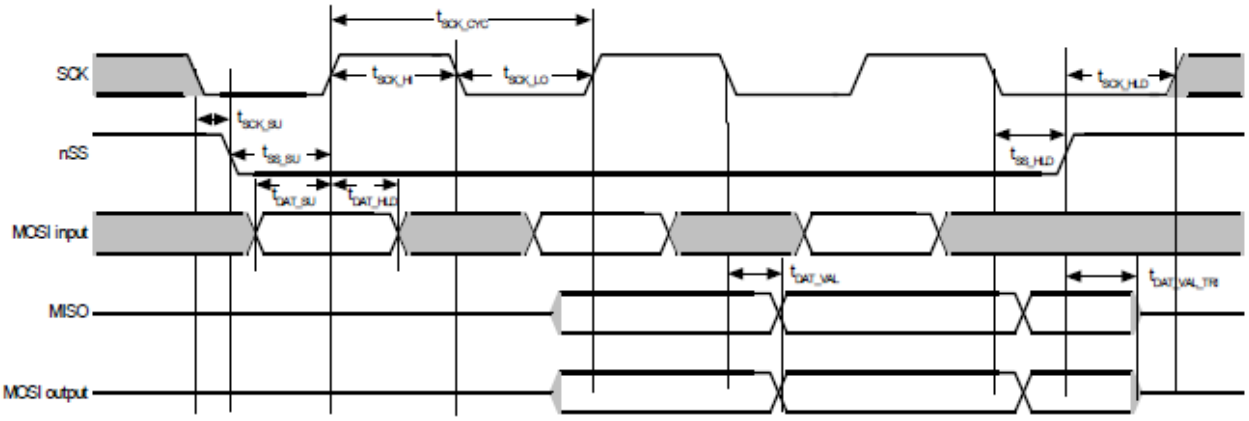


Figure 6 – SPI Timing

RF Characteristics

Parameter description	Conditions	Min.	Typ.	Max.	Unit
RF Frequency Range[2] [3]		2400		2497	MHz
Number of channels[2] [3]			98		
Channel bandwidth			1		MHz
Modulation Type			GFSK		
Receiver					
Sensitivity 125kbps	BER $1x10^{-3}$		-104		dBm
Sensitivity 250kbps	BER $1x10^{-3}$		-100		dBm
Sensitivity 1Mbps	BER $1x10^{-3}$		-91		dBm
Transmitter					
RF Power (E.R.P.) [4]	PA step 7	+18	+20	+22	dBm
RF Power (E.R.P.) [4]	PA step 6	+16	+18	+20	dBm
RF Power (E.R.P.) [4]	PA step 5	+14	+16	+18	dBm
RF Power (E.R.P.) [4]	PA step 4	+9	+11	+13	dBm
RF Power (E.R.P.)	PA step 0		-10		dBm
Power Management					
Crystal start to 10ppm			0.7	1.3	ms
Crystal start to IRQ	XSIRQ EN = 1		0.6		ms
Synth settle	Slow channels			270	us
Synth settle	Medium channels			180	us
Synth settle	Fast channels			100	us
Max packet length	All modes except 64-DDR			40	bytes
Max. packet length	64-DDR mode			16	bytes

[2]To be compliant with European ETSI standard requirements it is mandatory to use channels in the range from 2404MHz (channel 4) to 2480MHz (channel 80).

[3]To be compliant with USA FCC standard requirements it is mandatory to use channels in the range from 2401MHz (channel 1) to 2482MHz (channel 82).

[4]To be in compliance with the European ETSI standard requirements maximum output power level is 10mW. This condition is satisfied with step n°4 of 0x03 register. Instead to be in compliance with USA FCC standard there are no limits in power settings (step n°7 of 0x03 register may be used). Using step n°7 of that register, will obtained the max output power +20dBm.

Device usage

In order to obtain the performances described in the technical specifications and to comply with the operating conditions which characterize the Certification, the device must be mounted on a printed circuit taking into account the following:

Voltage Supply

1. The module must be powered by a low voltage safety source protected against short circuits. Maximum allowed voltage variations: 2.0÷3.6V.
2. Decoupling near the transmitter with a ceramic capacitor of at least 100.000 pF.

Ground:

It must surround in the best possible way the welding area of the transceiver. The ground plane should be made in the lower face and must not be present near the antenna integrated in order to avoid coupling.

Other components:

1. When mounting the module parallel to the PCB (XTR VF 2.4 HP/H-AI) do not include tracks near integrated antenna.
2. Keep the device away from all other components of the circuit (more than 5 mm)
3. Keep particularly far away and shielded all microprocessors and their clock circuits.