Figure 1

Contents

General description

The XTR EM 2.4 is a 1.5kbps to 72kbps low-power, low-voltage chip 2.4GHz ISM band RF transceiver ideal for battery operated wireless applications such as wireless sensors and control. The EM9209's built in custom low power micro-controller supports the proprietary wireless protocol links in the license-free 2.4000GHz to 2.4835GHz ISM band. It includes a low-IF receiver architecture and uses FSK modulation. A SPI interface provides a simple control of the baseband using an external host controller.

The EM9209 provides two communication modes with normal or high sensitivity and programmable bit rate from 1.5kbps to 72kbps. The EM9209 provides a divided clock output programmable at either 32.5kHz or 3.25MHz to drive external micro-controllers time reference.

Features

- Low voltage: 1,9 to 3,6 V
- Low power: 7mA in RX normal sensitivity mode (NS), 8mA in RX high sensitivity mode (HS).
- TX mode: 11mA at -1dBm, 36mA at +10dBm.
- < 150µA in stand-by mode.
- < 10nA in power down mode.
- High performance:
  - ➢ -115dBm sensitivity at 1.5kbps,
  - ➢ +10dBm maximum received input signal
  - ➢ Programmable output power from -20dBm to +10dBm

- Ultra compact radio design with low BOM cost:
  - ➢ COB with 4mm x 4mm footprint
- Operating temperatures: -40°C to +85°C
- Direct antenna interface (200Ω differential)
- Low-cost 26MHz crystal oscillator, frequency tolerance over temperature and aging of ±20ppm
- Flexible interface:
  - ➢ SPI interface for microcontrollers
  - ➢ Fully programmable link layer

Typical applications

- Remote sensing and control
- Wireless mice, keyboards, toys…
- Wireless watch sensors, sport equipment
- Alarm and security systems

XTR EM 2.4 pin out

VCC	2	1	GND
RESET	4	3	IRQ
SS	6	5	MOSI
MISO	8	7	SCK
EN	10	9	GND
NC	12	11	NC
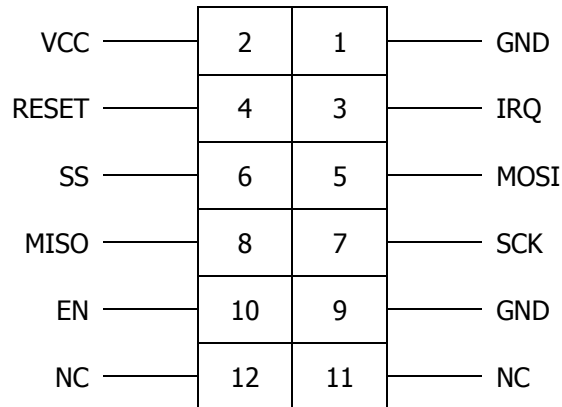
Figure 2

	Pin	Description
1	GND	GND connection.
2	VCC	Positive Voltage supply connection.
3	IRQ	Interrupt signal from the radio module.
4	RESET	Reset signal (active high) to the radio module.
5	MOSI	Master Out Slave In. SPI signal to the radio module.
6	SS	Slave Select signal (active high) to the radio module.
7	SCK	SPI clock to the radio module.
8	MISO	Master In Slave Out. SPI signal from the radio module.
9	GND	GND connection.
10	EN	Enable Pin.

Table 1 Pin description

Reference Documentation

The XTR EM 2.4 modules use the EM Microelectronic EM9209 Radio SOC device.
For information on technical details of the module such as register settings, timing, application interfaces and clocking refer to the device data sheet available on the website:
http://www.emmicroelectronic.com

Here below the link of the documentation:
http://www.emmicroelectronic.com/products/wireless-rf/proprietary-protocols/em9209

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European Reference Standards

The module **XTR EM 2.4** complies with the European standards **EN 300-228**, **EN 300-440** and **EN 301-489** with maximum power supply of 3.6V. The product has been tested according to EN 60950 and can be used inside a special housing that ensures compliance with the above mentioned regulations. The device must be powered by a low voltage safety source protected against short circuits.

The use of the module is foreseen inside housings that assure the overcoming of standards EN 61000 not directly applicable to the module itself. In particular, it is the user's care isolation antenna as the RF output of the transmitter is not able to support directly the electrostatic charges foreseen by the standard EN 61000-4-2.

Electrical Specifications

The device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken.

Parameters	Symbol	Min	Max	Unit
Supply Voltage	V_{BAT}	-0.3	3.8	V
Input Voltage	V_{IN}	$V_{ss} - 0,2$	$V_{BAT} + 0.2$	V
Electrostatic discharge	v_{ESD}	-1500	+1500	V
Maximum Soldering conditions		As per Jedec J-STD-020		

Table 2 Absolute maximum rating

General Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Supply Voltage V_{BAT}	V_{BAT}	1.9	2.5	3.6	V
Temperature Range	T_A	-40		+85	°C

Table 3 General Operating condition

Electrical Characteristics

Operating Mode	Notes	Symbol	Coditions	Min	Typ	Max	Unit
Power Down		I_{VBAT_PWDOWN}	EN_REG = 0			1	µA
Standby		I_{VBAT_STDBY}	26MHz crystal oscillator disabled		140		µA
Auto-calibration		$I_{AUTOCAL}$	Auto-calibration mode		4.2		mA
Transmit	1	I_{VBAT_TX3}	P_{OUT} = 1.1 dBm, 2440MHz		11		mA
		I_{VBAT_TX7}	P_{OUT} = 10 dBm, 2440MHz		36		mA
Receive	Normal sensitivity	I_{VBAT_RXNS}	2440 MHz		7		mA
	High sensitivity	I_{VBAT_RXHS}	2440 MHz		8		mA

Table 4 Supply currents on V_{BAT}
Note 1: See Table 9 for further clarifications

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Functional Overview
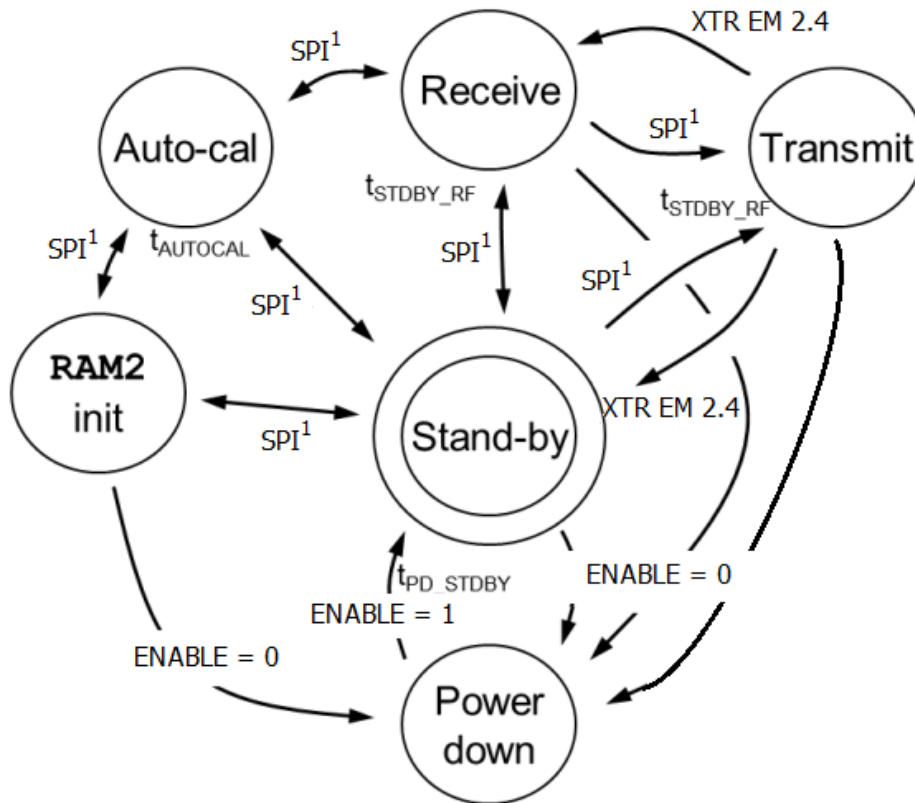
Figure 3 XTR EM 2.4 Functional Overview

Notes:
   1.   See SPI Communication chapter, page 6.

Power Down

This mode is enabled when ENABLE is tied to V_{SS} or left floating (3µA pull down). All regulators and the voltage reference are disabled and the supply current is in the nA range.

Standby Mode

When ENABLE is high the XTR EM 2.4 wakes up in standby mode at about $t_{PD-STBY}$ seconds (see Table 5). The SPI register memory is then set to 0 and it waits for new configuration. In standby mode all internal circuits are disabled and can be accessed.

RAM2 Init

The XTR EM 2.4 can be configured using a 16 registers memory RAM2. The RAM is resetted to 0 when ENABLE is set. In order to avoid 16 different write cycles, a dedicated subroutine located at ROM_BOOT_Address = 0 will initialize most RAM2 addresses to their default values.

Auto-cal

VCO center frequency
Due to temperature variations the XTR EM 2.4 frequency synthesizer has an auto calibration mode that must run periodically via SPI command; this procedure assures that the FSK modulator is kept operating and whitin specification. Tipically, an auto calibration procedure should be run when a changing channel or a temperature variation (more than 10°C) occurs.

PTAT reference current
The internally generated PTAT current can be self calibrated using an internal PTAT generator.

Transmit

During the transmission routine the XTR EM 2.4 outputs a FSK-modulated packet, it returns to receive mode or standby mode with the crystal oscillator enabled and sets the interrupt pin IRQ high. Depending on the subroutine previously set (in the RAM2 Init procedure) the XTR EM 2.4 can transmit the whole TXFIFO (till TXFIFO size is 0) or a predefined number of bytes programmed in RAM2.
Transmit operation can be set using the SPI command Send_TXFIFO.

Receive

The XTR EM 2.4 in receive mode waits for a FSK-modulated packet. After receiving a suitable packet it sets the IRQ pin high. Depending on the programmed subroutine, it can either read the size of the packet to be received in the header or in RAM2.

Parameter	Notes	Symbol	Min	Typ	Max	Unit
Standby mode → TX/RX mode	1	$t_{STBY-RF}$	0.8	1	10	ms
Power Down → Standby mode		$t_{PD-STBY}$	1000			µs
Auto calibration		$T_{AUTOCAL}$	340			µs

Table 5 Timing characteristics (VBAT = 2.5V)

Note 1: Dominated by the crystal oscillator startup time, which strongly depends on the quartz Q-factor.

SPI Communication

The XTR EM 2.4 has an SPI interface supporting communication between an application microcontroller and one or more slave devices with the SPI standards. The SPI interface is used to read from and to write into all the registers.

SPI operations allow various accesses:
- Memories write and read actions
- Micro-controller commands
- Loading of subroutines in RAM1
- Test instructions (used in production)

A SPI transaction is defined as all of the activity on SCK, MOSI and MISO that occurs between one rising edge of SS and its next falling edge. All the data shall be sent starting with the MSB first.
Not all the commands are encoded on a number of bits multiple of 8. Additional clocks can be sent after the command with no impact on the command decoding. Thus, the chip can be accessed without problems

using an 8-bit wide SPI interface. Each change to MOSI is latched on the rising edge of SCK, and each change to MISO is available on the falling edge of SCK. A timing diagram is shown in Figure 4. Complete timing specifications are given in Table 6.
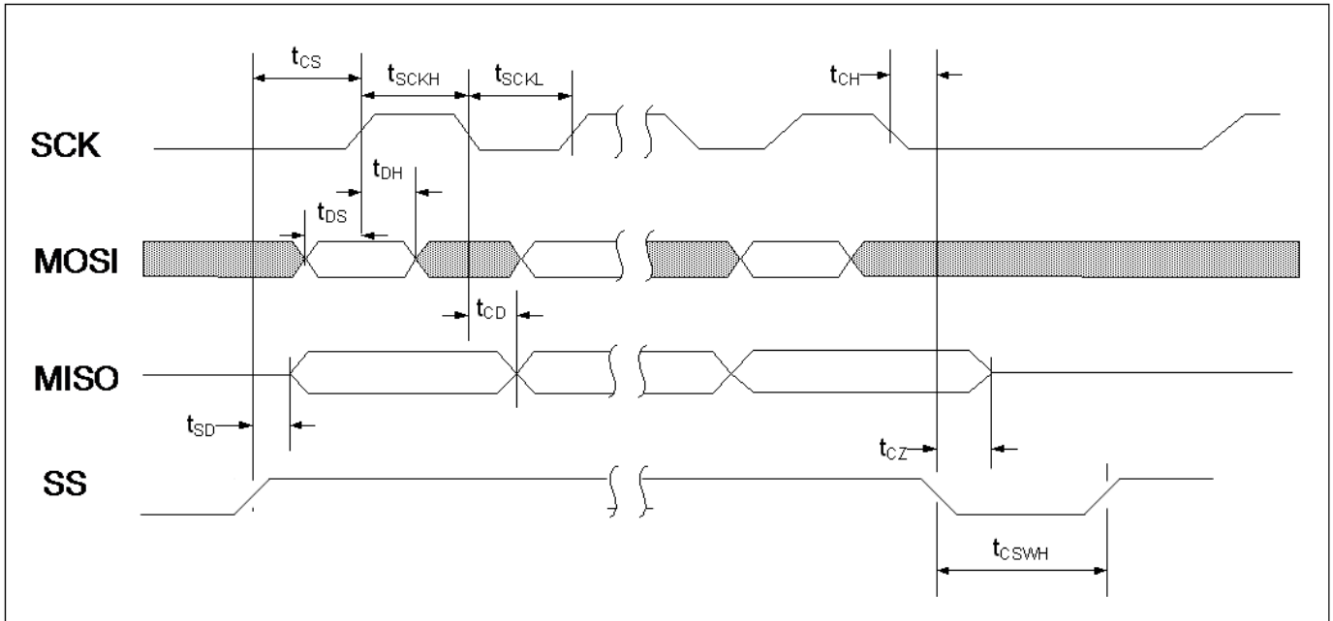
Figure 4 SPI timing diagram

Symbol	Parameters	Min	Max	Units
t_{DS}	MOSI to SCK Setup	20		ns
t_{DH}	SCK to MOSI hold	20		ns
t_{SD}	SS to MISO Valid		30	ns
t_{CD}	SCK to MISO Valid		30	ns
t_{SCKL}	SCK low time	40		ns
t_{SCKH}	SCK high time	40		ns
f_{sck}	SCK frequency	0	10	MHz
t_{CS}	SS to SCK Setup	20		ns
t_{CH}	SCK to SS Hold	20		ns
t_{CSWH}	SS Inactive Time	20		ns
t_{CZ}	SS to MISO High Z		30	ns

Table 6 SPI timing values   **Condition: 25°C, 2.5V, 25pF**

For each SPI command, MISO will always give three status bits on the first three SCK cycles.
- As soon as SS goes high, the first status bit (Status[2]) is available on the MISO terminal. This bit is called "Previous_FIFO_Order_Pending" and is high when the microcontroller has not yet processed the previous FIFO order. This process takes a maximum of 8 clock cycles and starts on the falling edge of the SS signal.
- Status[1] reflects the inactivity of the crystal oscillator (0: running).
- Status[0] shows the unlock state of the 2.4GHz LO frequency synthesizer (0: main LO PLL locked).

For connect transmission operation, status[2..0] must be equal to '000'.

SPI Commands

- *Read_RXFIFO*

MOSI	1	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x
MISO	Status[2..0]			RXFIFO_Size[4..0]					RXFIFO_Data[7..0]							

This command returns the next byte out of the RXFIFO. It also returns the total number of bytes currently available in the RXFIFO (including the one being read).

This SPI operation works together with the internal microcontroller and is functional only when this latter has been started (SPI command Start_Micro) and when the master clock is active (Crystal oscillator must be enabled). The order is taken into account only when SS signal goes down and the RXFIFO size information are sampled when SS is low.
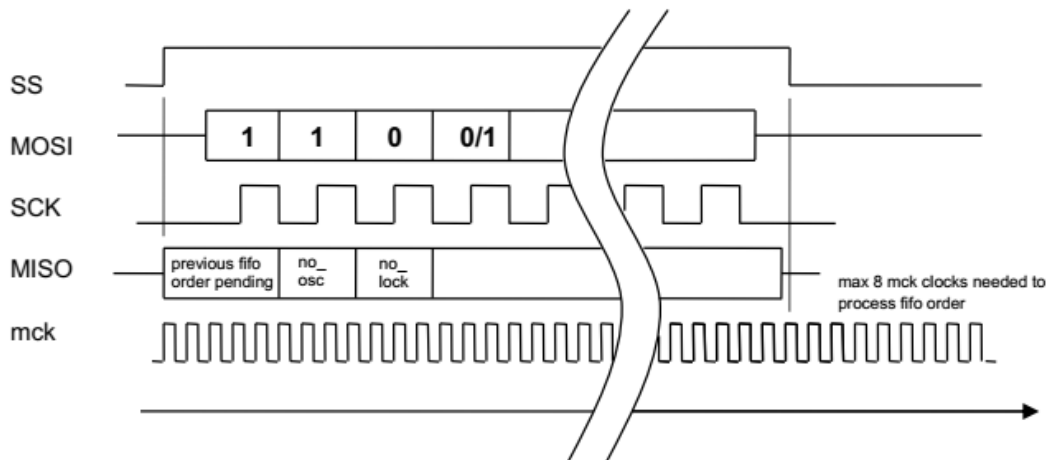
Figure 5 Timing of the SPI Read_RXFIFO / Write_TXFIFO command

- *Write_TXFIFO*

MOSI	1	1	0	1	TXFIFO_Data[7..0]								x	x	x	x
MISO	Status[2..0]			RXFIFO_Size[4..0]					TXFIFO_Size[4..0]					x	x	x

This command writes a byte to the TXFIFO. It also returns the total number of bytes in both FIFOs, not including this one. This SPI operation works together whit the internal microcontroller and is functional only when this latter has been started (SPI command Start_Micro) and when the master clock is active (Crystal oscillator must be enabled). The order is taken into account only when SS signal goes down and the FIFO size information are sampled by mck when SS is low.

- *Read_RXFIFO_Size*

MOSI	1	1	1	0	0	0	0	x	x	x	x	x	x	x	x	x
MISO	Status[2..0]			x	x	x	x	RXFIFO_Size[4..0]					x	x	x	x

This command reads the total number of bytes currently available in the RXFIFO.

- *Read_TXFIFO_Size*

MOSI	1	1	1	0	0	0	1	x	x	x	x	x	x	x	x	x
MISO	Status[2..0]			x	x	x	x	TXFIFO_Size[4..0]					x	x	x	x

This command reads the total number of bytes currently available in the TXFIFO.

- *Read_RAM1*

MOSI	0	0	1	address[5..0]						x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	Status[2..0]			x	x	x	x	x	x	data_read[11..0]												x	x	x

This command reads the 12 bits word from the specified address (6bits) of RAM1. This command will put the microcontroller on hold and reset state, until last bit has been processed.

- *Write_RAM1*

MOSI	0	0	0	address[5..0]						data_write[11..0]												x	x	x
MISO	Status[2..0]			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

This command writes a 12 bits word to the specified address (4 bits) of RAM1. This command will put the microcontroller on hold and reset state until last bit has been processed.

- *Read_RAM2*

MOSI	0	1	1	address[3..0]				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	Status[2..0]			x	x	x	x	data_read[11..0]												x	x	x	x	x

This command reads the 12 bits word to the specific address (4 bits) of RAM2. This command will put the microcontroller on hold until last bit has been processed.

- *Write_RAM2*

MOSI	0	1	0	address[3..0]				data_write[11..0]												x	x	x	x	x
MISO	Status[2..0]			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

This command writes a 12 bits word to the specified address (4 bits) of RAM2. This command will put the microcontroller on hold until last bit has been processed.

- *Reset_Micro*

MOSI	1	1	1	0	0	1	0	x
MISO	Status[2..0]			x	x	x	x	x

This instruction allows an asynchronous reset of the microcontroller. Never use this command when the micro is running (RAM2 and FIFO's content could be corrupted). Always first stop the micro using SPI command Stop_Micro prior to use Reset_Micro.

- *Stop_Micro*

MOSI	1	1	1	0	0	1	1	x
MISO	Status[2..0]			x	x	x	x	x

This command stops the microcontroller.

- *Start_Micro*

MOSI	1	1	1	0	1	0	0	x
MISO	Status[2..0]			x	x	x	x	x

This command start the microcontroller and executes the program currently stored in RAM1.

- *Clear_IRQ*

MOSI	1	1	1	0	1	0	1	x
MISO	Status[2..0]			x	x	x	x	x

Use this command to reset the IRQ signal. It works only when microcontroller is running.

- *Send_TXFIFO*

MOSI	1	1	1	0	1	1	0	x
MISO	Status[2..0]			x	x	x	x	x

This command will send the current contents of the TXFIFO. Depending on the selected subroutine, the program either sends the full content of the FIFO, or the number of bytes specified in RAM2.

- *Aux_com*

MOSI	1	1	1	0	1	1	1	x
MISO	Status[2..0]			x	x	x	x	x

This command allows the Channel RSSI to be read and stored to Limit_RSSI[3:0].

- *ROM_Boot*

MOSI	1	1	1	1	0	0	0	ROM_Boot_Address[8..0]									
MISO	Status[2..0]			x	x	x	x	x	x	x	x	x	x	x	x	x	x

This command copies the 64 12 bits instructions from the specified ROM address to RAM1. This allows for fast initialization of the microcontroller subroutines.
The crystal oscillator must be enabled to perform this operation. Additionally, ROM_Boot command stops and resets the microcontroller.

- *ROM_Boot0_and_Start*

MOSI	1	1	1	1	1	1	1	x
MISO	Status[2..0]			x	x	x	x	x

This command copies the 64 12-bits instructions from the ROM address 0 to RAM1. This allows for fast initialization of the microcontroller subroutines.
The crystal oscillator must be enabled to perform this operation. Additionally, ROM_Boot0_and_Start command resets and starts the microcontroller. It goes in standby mode.

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RAM2 Registers

In this section are shown all the most relevant RAM2 Register in order to properly configure the XTR EM 2.4.

0	Bit position	11	10	9	8	7	6	5	4	3	2	1	0
	Default Value	1	1	1	1	1	1	0	0	0	1	0	0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
	Description	VDD_Synth _En	VDD_RXTX _En	Xtal_En	Reserved					Div_Ck_Freq[0]	Div_Ck_Freq[1]	Reserved	
		Voltage Regulator Enable	Voltage Regulator Enable	Crystal Oscillator Enable	Reserved					Select the frequency of the clock output on DIV_CK (see test point)		Reserved	

1	Bit position	11	10	9	8	7	6	5	4	3	2	1	0
	Default Value	0	0	0	0	0	0	0	0	0	0	0	0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
	Description	Reserved									TX_On	RX_On	Reserved
		Voltage Regulator Enable	Voltage Regulator Enable	Crystal Oscillator Enable	Reserved				Select the frequency of the clock output on DIV_CK (see test point)		Reserved		

2	Bit position	11	10	9	8	7	6	5	4	3	2	1	0
	Default Value	1	0	1	0	0	0	0	1	0	1	0	1
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
	Description	Reserved											
		Reserved											

3	Bit position	11	10	9	8	7	6	5	4	3	2	1	0
	Default Value	0	0	1	0	1	1	0	0	1	0	0	0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
	Description	Reserved								VCO_Code [3]	VCO_Code [2]	VCO_Code [1]	VCO_Code [0]
		Reserved								The VCO tuning code is determined automatically by auto-calibration procedure			

4	Bit position	11	10	9	8	7	6	5	4	3	2	1	0
	Default Value	0	1	1	0	1	0	0	0	0	0	0	0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
	Description	I_Pre_PA [4]	I_Pre_PA [3]	I_Pre_PA [2]	I_Pre_PA [1]	I_Pre_PA [0]	Reserved						
		Current bias of the PA preamplifier. Defines RF Output power in TX mode					Reserved						

5	Bit position	11	10	9	8	7	6	5	4	3	2	1	0
	Default Value	0	1	0	0	0	1	0	0	1	0	0	0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
	Description	Reserved								Main_PTAT [3]	Main_PTAT [2]	Main_PTAT [1]	Main_PTAT [0]
		Reserved								Control of the main chip PTAT current bias			

6

Bit position	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	1	0	1	1	0	0	0	0	0	0	0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
Description	I_PA [4]	I_PA [3]	I_PA [2]	I_PA [1]	I_PA [0]	Reserved						
	Current bias of the PA. Defines RF Output Power in Transmit mode					Reserved						

7

Bit position	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	1	0	0	1	0	0	0	0	0	0	0	0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
Description	Reserved											
	Reserved											

8

Bit position	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	1	0	0	1	0	0	0	0	0	0	0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
Description	Reserved						RB_Inst_Dis	Reserved	Limit_RSSI [3]	Limit_RSSI [2]	Limit_RSSI [1]	Limit_RSSI [0]
	Reserved						ROMBoot Instruction Disable	Reserved	RSSI Value			

9

Bit position	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	1	0	1	0	0	0	0	0	0	0	0	0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
Description	Reserved				DFT_Mes [7]	DFT_Mes [6]	DFT_Mes [5]	DFT_Mes [4]	DFT_Mes [3]	DFT_Mes [2]	DFT_Mes [1]	DFT_Mes [0]
	Reserved				Error frequency measured by DFT in High Sensitivity mode							

10

Bit position	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	1	1	0	0	0	0	0	0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
Description	Reserved											
	Reserved											

11

Bit position	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	1	1	0	0	0	0	0	0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
Description	Reserved											
	Reserved											

12	Bit position	11	10	9	8	7	6	5	4	3	2	1	0
	Default Value	0	0	0	1	1	0	0	0	0	0	0	0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
	Description	Ch_Rate[2]	Ch_Rate[1]	Ch_Rate[0]	R_Bit_Ck [8]	R_Bit_Ck [7]	R_Bit_Ck [6]	R_Bit_Ck [5]	R_Bit_Ck [4]	R_Bit_Ck [3]	R_Bit_Ck [2]	R_Bit_Ck [1]	R_Bit_Ck [0]
		Bandwidth of the normal sensitivity demodulator			CODEC Bit clock frequency								

13	Bit position	11	10	9	8	7	6	5	4	3	2	1	0
	Default Value	0	0	0	0	1	0	1	0	1	0	0	1
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
	Description	Reserved				Address[7]	Address[6]	Address[5]	Address[4]	Address[3]	Address[2]	Address[1]	Address[0]
		Reserved				Address Byte Value							

14	Bit position	11	10	9	8	7	6	5	4	3	2	1	0
	Default Value	0	0	0	1	1	1	0	0	0	0	1	1
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
	Description	Reserved		Frequ[4]	Frequ[3]	Frequ[2]	Frequ[1]	Frequ[0]	N_Pay[4]	N_Pay[3]	N_Pay[2]	N_Pay[1]	N_Pay[0]
		Reserved		Synthesizer's RF Frequency LSB's					Payload size of the Packet: N_Pay + 1				

15	Bit position	11	10	9	8	7	6	5	4	3	2	1	0
	Default Value	0	1	1	1	0	1	1	0	0	0	1	0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0
	Description	Frequ[16]	Frequ[15]	Frequ[14]	Frequ[13]	Frequ[12]	Frequ[11]	Frequ[10]	Frequ[9]	Frequ[8]	Frequ[7]	Frequ[6]	Frequ[5]
		Synthesizer's RF Frequency MSB's											

Channel Data Rate

The XTR EM 2.4 has a programmable channel data rate, it varies from 1.5kbps to 72kbps in normal sensitivity mode and from 1.5kbps to 12kbps for high sensitivity mode.

On air bit rate [kbps]	Ch_Rate[2:0]	R_Bit_Ck[8:0]	RAM2@12 [11:0]
1.5	000	110000000	0x180
2.99	001	011000000	0x2C0
6.02	010	001011111	0x45F
12.037	011	000101111	0x62F
24.074	100	000010111	0x817
48.15	101	000001011	0xA0B
72.22	110	000000111	0xC07

Table 7

RF Characteristics

Parameter description		Min.	Typ.	Max.	Unit
RF Frequency Range		2400		2484	MHz
Number of channels			20		
Channel bandwidth			1		MHz
Channel spacing			4		MHz
Modulation Type			FSK		
Receiver					
Sensitivity for 0.1% BER at room temperature	High (1.5 kbps)		-115		dBm
	High (3 kbps)		-113		dBm
	High (6 kbps)		-111		dBm
	High (12 kbps)		-107		dBm
	Normal (24 kbps)		-100		dBm
	Normal (48 kbps)		-98		dBm
	Normal (72 kbps)		-97		dBm
Maximum input power for 0.1% BER	High		-10		dBm
	Normal		-10		dBm
Transmitter					
Power Level	Current Consumption [mA]		Output Power		
7	36.3		+10		dBm
6	29.5		+9.3		dBm
5	20.7		+6.6		dBm
4	14.4		+2.7		dBm
3	11.2		-1.1		dBm
2	10.2		-3.1		dBm
1	8.1		-10.4		dBm

Table 8 RF Characteristics

TX Power Level

Power Level	I_Pre_PA[4:0] [unsigned decimal]	I_PA[4:0] [unsigned decimal]	Output Power [dBm]	PA Power Efficiency [%]	DC total current consumption [mA]
7	29	18	+10	27.3	36.3
6	21	5	+9.3	29.7	29.5
5	10	2	+6.6	24.2	20.7
4	7	1	+2.7	15.8	14.4
3	4	1	-1.1	9.4	11.2
2	3	1	-3.1	7	10.2
1	1	1	-10.4	1.9	8.1

Table 9 RF Power Settings

Aurel catalogue

Aurel Code	Technical name reference	Description
650201476G	AUREL XTR-EM-2.4	2.4 GHz module
65PR02532*	AUREL DB-XTR-EM-2.4	2.4 GHz demoboard

* this Aurel code will be subject to a revision when further development will be available.

Revision History

Date	Description	Revision
-/-/2019	First Release	-